2000-227324

[Name of Document]	PATENT APPLICATION
[Reference Number]	A000004168
[Filing Date]	July 27, 2000
[To]	Commissioner, Patent Office
[International Patent Classification]	H01L 21/00
[Title of the Invention]	METHOD AND SYSTEM FOR PRODUCING SEMICONDUCTOR DEVICES
[Number of Claims]	8
[Inventor]	
[Address or Residence]	8 Sinsugita-cho, Isogo-ku, Yokohama-shi, Kanagawa c/o Yokohama Complex of KABUSHIKI KAISHA TOSHIBA
[Name]	Ryoichi Inanami
[Inventor]	
[Address or Residence]	8 Sinsugita-cho, Isogo-ku, Yokohama-shi, Kanagawa c/o Yokohama Complex of KABUSHIKI KAISHA TOSHIBA
[Name]	Shunko Magoshi
[Inventor]	
[Address or Residence]	1 Komukaitoshiba-cho, Saiwai-ku, Kawasaki-shi, Kanagawa c/o Yokohama Complex of KABUSHIKI KAISHA TOSHIBA
[Name]	Katsuya Okumura
[Applicant for Patent]	
[Identification Number]	000003078
[Name]	KABUSHIKI KAISHA TOSHIBA

[Agent]	
[Identification Number]	100058479
[Patent Attorney]	
[Name]	Takehiko Suzuye
[Phone Number]	03-3502-3181
[Appointed Agent]	
[Identification Number]	100084618
[Patent Attorney]	
[Name]	Sadao Muramatsu
[Appointed Agent]	
[Identification Number]	100068814
[Patent Attorney]	
[Name]	Atsushi Tsuboi
[Appointed Agent]	
[Identification Number]	100092196
[Patent Attorney]	
[Name]	Yoshiro Hashimoto
[Appointed Agent]	
[Identification Number]	100091351
[Patent Attorney]	
[Name]	Akira Kohno
[Appointed Agent]	
[Identification Number]	100088683
[Patent Attorney]	
[Name]	Makoto Nakamura

[Appointed Agent]		
[Identification Number]	100070437	
[Patent Attorney]		
[Name]	Shoji Kawai	
[Indication of Official Fee]		
[Prepayment Register Number]	011567	
[Amount of Payment]	¥21,000.-	
[List of Items submitted]		
[Name of Item]	Specification	1
[Name of Item]	Drawing	1
[Name of Item]	Abstract	1
[Necessity of Proof]	Necessary	

[Document] SPECIFICATION

[Title of the Invention] METHOD AND SYSTEM FOR PRODUCING SEMICONDUCTOR DEVICES

[What is claimed is:]

[Claim 1] A method of producing a semiconductor device upon receiving an order for the semiconductor device by transmitting/receiving information between a person who wishes to receive an order and a person who wishes to place an order through a network, the method characterized by comprising:

a first step of causing the person who wises to place an order to input specifications of the semiconductor device by request of the person who wishes to place an order;

a second step of generating a plurality of circuit patterns in consideration of conditions for transferring a pattern by charged-particle beam exposure of a character projection method based on the specifications of the semiconductor device selected by the person who wishes to place an order, and obtaining at least two design parameters for each of the circuit patterns; and

a third step of presenting the at least two design parameters to the person who wishes to place an order for each of the circuit patterns and causing the person who wishes to place an order to select a circuit pattern satisfying a desired condition.

[Claim 2] The method according to claim 1, characterized in that a cost and a delivery time period for each of the circuit patterns are calculated in the second step, and the cost and the delivery time period are presented to the person who wishes to place an order in the third step.

[Claim 3] The method according to claim 2, characterized in that the cost includes a production cost of a CP aperture to be newly produced by the charged-particle beam exposure of the character projection method, and the delivery time period includes a production time period required for newly producing a CP aperture.

[Claim 4] The method according to claim 1, characterized by comprising: a fourth step of requesting a device maker to generate the selected circuit pattern through the network after the third step.

[Claim 5] The method according to claim 1, characterized by comprising: a fourth step of requesting a CP aperture maker to produce a CP aperture necessary for generating the selected circuit pattern through the network after the third step.

[Claim 6] A system for producing a semiconductor device through a network, characterized by comprising:

a standard cell library which is configured to store a plurality of standard cells for optimizing a circuit pattern for each functional unit;

a CP aperture library which is configured to store a plurality of CP apertures as design data, the CP apertures being used for charged-particle beam exposure of a character projection method;

a condition setting section which is configured to cause a person who wishes to place an order to input specification of the semiconductor device through the network;

a circuit pattern generating section which is configured to generate a plurality of circuit patterns based on the specifications using the standard cells stored in the standard cell library;

a parameter calculating section which is configured to calculate at least two design parameters for the plurality of circuit patterns generated from the circuit pattern generating section; and

a circuit pattern selecting section which is configured to present the at least two design parameters to the person who wishes to place an order through the network and causing the person to place an order.

[Claim 7] The system according to claim 6, characterized in that the parameter calculating section further calculates a cost and a delivery time period for each of the plurality of circuit patterns, and

the circuit pattern selecting section presents the cost and the delivery time period to the person who wishes to place an order.

[Claim 8] The system according to claim 7, characterized in that the cost includes a production cost of a CP aperture to be newly produced by the charged-particle beam exposure of the character projection method, and the delivery time period includes a production time period required for newly producing a CP aperture.

[Detailed Description of the Invention

[0001]

[Technical Field of the Invention]

The present invention relates to a method for producing a semiconductor device by charged-particle beam exposure using a character projection (CP) method and a system for producing the semiconductor device.

[0002]

[Prior Art]

Electron-beam exposure is an effective means for processing a fine pattern of a semiconductor circuit.

[0003]

In a variable shaped beam (VSB) method that is a typical electron-beam exposure method, a circuit pattern is divided into very small rectangles and triangles and these are repeatedly exposed to an electron beam. It is thus unnecessary to prepare a mask dedicated to the exposure of the pattern. However, a very large number of shots of the electron beam are required and thus a reduction in throughput is inevitable.

[0004]

A character projection (CP) method is contrived in order to improve the throughput of the VSB method. In the CP method, the electron beam is formed to characters within a maximum size of the beam, and the characters are exposed by the electron beam at once, thereby reducing the number of shots of the beam and improving the throughput. The electron beam is formed by a character-shaped CP aperture. In a commonly used electron-beam exposure apparatus, the number of apertures that can be formed in a deflection region of a character-selecting deflector is 100 at the most. In a device which has a number of same patterns which are used repeatedly such as a memory, most of the patterns can be exposed by the CP method. In a logic device such as an ASIC (application-specific integrated circuit), the number of types of characters used repeatedly is as large as several hundreds to several thousands. The VSB method is therefore used more frequently than the CP method to expose the characters. If the VSB method is increased in use, the effect of reducing the number of shots, which is created by adopting the CP method, is lessened naturally; therefore, a high throughput cannot be achieved. Since a CP aperture is required for each product, manufacturing costs cannot be decreased, nor can be time periods.

[0005]

In producing a logic device as described above, especially a circuit pattern designed on the basis of standard cells (SC), a logic synthesis method and an P & R (Place and Route) method are proposed, which greatly reduces the number of SCs serving as characters when electron-beam exposure is performed by the CP method or which the number of standard cells for use is restricted. According to these methods, the performance of the predetermined circuit pattern slightly deteriorates and the area of a chip slightly decrease. However, the number of shots of electron-beam exposure can be reduced and the number of characters for exposure of the CP method can be made equal to or smaller than that of characters, which can be prepared by an exposure apparatus. The same CP aperture can be used for different logic devices. A mask or a CP aperture need not be produced for each product, with the result that manufacturing costs and periods can be cut out.

[0006]

According to the above design method, a plurality of patterns can be generated for desired device specifications. The most desirable pattern can thus be selected in terms of costs, delivery times, and capabilities. For example, the following five conditions are provided as pattern selection criteria in this case: 1) The number of shots of electron beam is the smallest or the throughput of exposure is the highest; 2) Electron-beam exposure is performed using a previously formed CP aperture, that is, the costs and periods of manufacturing the CP aperture can be cut out; 3) The chip area of a device to be manufactured is the smallest; 4) The power consumption of a device to be manufactured is the lowest; and 5) The operating frequency of a device to be manufactured is the highest. It is preferable that a person who makes a request to manufacture a device, i.e., a user or a customer of a semiconductor manufacturer decides which condition is prioritized and a logic device of what circuit pattern is produced.

[0007]

A conventional process from the design of a circuit pattern of a semiconductor device to the electron-beam exposure will now be described with reference to the flowchart shown in FIG. 10.

[0008]

As FIG. 10 shows, an electronic circuit of the semiconductor device is described first (s101). It is usually described using hardware description language (HDL). In particular, register transfer level (RTL) is employed to describe the arrangement and operation of registers and those of register-to-register logic circuits.

[0009]

Then, logic synthesis is performed based on device characteristics such as the RTL and an operating frequency and design limiting conditions such as a chip area (s102). A logic circuit satisfying the design limiting conditions can thus be obtained. A circuit pattern is formed on the basis of the logic circuit. A functional unit such as a logic gate and a flip-flop is assigned to standard cells for optimizing a circuit pattern. These standard cells are arranged on a chip and connected to each other by wiring. This arrangement is called P & R (Place and Route).

[0010]

After that, various verifications are performed to generate pattern data of the device (s103).

[0011]

The above steps s101 to s103 are carried out by a designer of the circuit pattern.

[0012]

The step s104 and its subsequent steps are performed by a process engineer as follows.

[0013]

First, an operator receives pattern data from the designer of the circuit pattern (s104) and extracts figures, which serves as characters for CP exposure or is used repeatedly, from the figures contained in the pattern data. The extracted figures are assigned to the characters for CP exposure, while the number of characters mountable on an exposure apparatus is set as a limit value (s105). The other figures are exposed by the VSB method.

[0014]

A CP aperture is prepared for the characters to which the figures are assigned (s106). Based on information of steps s104 and s105, design information is converted to exposure data that can be put to an electron-beam exposure apparatus using pattern data (s107). The CP aperture formed in step s106 is attached to the exposure apparatus. The exposure data generated in step s107 is input to the exposure apparatus, and a sample is exposed to an electron beam (s108). The completely exposed sample is removed from the exposure apparatus and then heated and developed to form a resist pattern (s109).

[0015]

[Object of the Invention]

In the foregoing techniques of designing a circuit pattern and exposing the pattern to an electron beam, the steps s101 to s103 are usually carried out by a designer of the circuit pattern, while the steps s104 to s109 are performed by a process engineer. It is not one person but a plurality of persons of different types who are in charge of the respective steps. The designer designs a circuit pattern without considering any characters in the electron-beam exposure of the CP method. On the other hand, the process engineer extracts figures as a unit of the CP exposure from the pattern data generated by the designer and assigns it to the characters. However, the designer cannot take into consideration all the contents that are subject to constraints in terms of a process.

Consequently, the designer and engineer are satisfied with the parameters for the process and design, but they have no other choice but to take a very inefficient exposure method for the other parameters. This leads to the design and exposure method that do not necessarily meet the user's needs in manufacturing a semiconductor device. More specifically, when a user instructs a semiconductor-device maker to manufacture a semiconductor device performing a desired operation, the designer selects a circuit pattern that satisfies the optimum design condition based on the operation. Then, the process engineer makes the exposure device expose the circuit pattern selected by the designer which is made by an electron beam. The above process therefore has the problem that the manufacturing costs and periods required eventually for the production cannot meet the needs of a user. In other words, though the above five conditions 1) to 5) are provided as pattern selection criteria, the user's pattern selection is substantially based on very limited parameters for design.

[0016]

The present invention has been made in order to solve the above-described requirements, and it is an object of the invention to provide a method which can efficiently produce a semiconductor device that fills the user’s needs, and a system for producing the semiconductor device.

[0017]

[Means for Achieving the Object]

According to an aspect of the present invention, there is provided a method of producing a semiconductor device upon receiving an order for the semiconductor device by transmitting/receiving information between a person who wishes to receive an order and a person who wishes to place an order through a network, the method characterized by comprising: a first step of causing the person who wises to place an order to input specifications of the semiconductor device by request of the person who wishes to place an order; a second step of generating a plurality of circuit patterns in consideration of conditions for transferring a pattern by charged-particle beam exposure of a character projection method based on the specifications of the semiconductor device selected by the person who wishes to place an order, and obtaining at least two design parameters for each of the circuit patterns; and a third step of presenting the at least two design parameters to the person who wishes to place an order for each of the circuit patterns and causing the person who wishes to place an order to select a circuit pattern satisfying a desired condition.

[0018]

The specifications of semiconductor devices represent conditions for specifying the semiconductor devices when a person receives an order for the semiconductor devices before logic synthesis and P & R are performed. The conditions include design parameters such as an operating frequency, a chip area, and power consumption.

[0019]

The design parameters include parameters such as manufacturing costs and delivery time periods, which are referred to as conditions for receiving an order for semiconductor devices, as well as parameters necessary for designing a semiconductor device, such as an operating frequency, a chip area, power consumption, throughput, the number of shots, and the number of CP apertures for use. In other words, the design parameters are all the parameters used for determining whether a person receives an order or not.

[0020]

With the configuration described above, a person who wishes to place an order making a request to produce a semiconductor device can directly contact a person who wishes to receive an order through the network and generates a circuit pattern of a desired device by simulation. In this case, the parameters such as the performance of a device, the area of a chip, and the manufacturing costs and periods, which are required by the person who wishes to place an order as a criterion of determination for making a request to produce a device, are presented to and selected by the person who wishes to place an order. The person who wishes to place an order can thus select and order the most suitable pattern without causing a difference in consciousness among the designer, process engineer, and the person who wishes to place an order. More specifically, though the performance of the device is slightly degraded, a pattern that allows the device to be produced inexpensively and quickly can be selected.

[0021]

Further, a manufacturing period, which varies with whether an existing CP aperture can be used for electron-beam exposure, can correctly be estimated. Since the use of the existing CP aperture is taken into consideration, the cost and period for manufacturing the CP aperture can be omitted, and the cost can be prevented from increasing even when a small number of devices are produced.

[0022]

Since, moreover, the person who wishes to receive an order can place an order with a semiconductor maker and a CP aperture maker in real time, the manufacturing period can be shortened.

[0023]

Desirably a cost and a delivery time period for each of the circuit patterns are calculated in the second step, and the cost and the delivery time period are presented to the person who wishes to place an order in the third step. Accordingly, not only the design parameters of the semiconductor device but also the parameters almost fulfilling the needs of the person who wishes to place an order can be used as a criterion of pattern determination, which can realize a higher customer satisfaction level.

[0024]

Desirably the cost includes a production cost of a CP aperture to be newly produced by the charged-particle beam exposure of the character projection method, and the delivery time period includes a production time period required for newly producing a CP aperture. Therefore, when the charged-particle beam exposure using the character projection method is carried out, the person who whishes to place an order receives the production time periods and costs required for an existing

CP aperture and required for the newly producing CP aperture as a criterion of determination for pattern selection. As a result, the person who wishes to place an order can select a pattern by accurately grasping the condition of the person who wishes to receive an order. In addition, since the mask producing cost and period can be omitted, even a small production can restrain the cost from increasing, making it possible to produce a semiconductor device which meets the individual needs of persons who wish to place an order.

[0025]

Desirably included is a fourth step of requesting a device maker to generate the selected circuit pattern through the network after the third step. Further, included is a fourth step of requesting a CP aperture maker to produce a CP aperture necessary for generating the selected circuit pattern through the network after the third step. Thus, the person who wishes to receive an order can directly request a factory of the device maker or CP aperture maker to produce a semiconductor device simultaneously upon receiving an order. This allows the semiconductor device according to the user's wish to be speedily produced.

[0026]

The present invention is also realized as a semiconductor-device producing system for achieving the above method.

[0027]

[Embodiment of the Invention]

An embodiment of the present invention will now be described with reference to the accompanying drawings.

[0028]

(First Embodiment)

FIG. 1 is a block diagram showing a network structure of a semiconductor-device production system according to a first embodiment of the present invention. This production system includes a server 1 as a system operator for operating the production system as a person who wishes to receive an order, a user terminal 2 used by a plurality of users for using the production system as a person who wishes to place an order, an aperture maker terminal 3 used by an aperture maker who produces apertures based on an order by the server 1, a device maker terminal 4 used by a device maker who produces devices based on an order by the server 1, and a network 5. The server 1, user terminal 2, aperture maker terminal 3, and device maker terminal 4 are connected to the network 5. The network connection can be established by wire or radio. Further, the server 1 can directly be connected to an exposure control computer for controlling an exposure apparatus installed in a factory of the device maker or the aperture maker, not through the network 5 but through a private line.

[0029]

FIG. 2 shows an example of the server 1 in detail. Referring to FIG. 2, an interface 11 for communicating data with the network 5 is connected to a processor 12 for processing various data items. The processor 12 is connected to a cell library 13 and a CP aperture library 14. The CP aperture library 14 can directly be connected to the above exposure control computer installed in a factory of the device maker or the aperture maker via a private line.

[0030]

The processor 12 includes a condition setting section 12a, a circuit pattern generating section 12b, and a circuit pattern selecting section 12c. The condition setting section 12a causes a user to input or select operations and specifications of a semiconductor device to set basic conditions for forming a circuit pattern. The circuit pattern generating section 12b generates a plurality of circuit patterns based on the operations and specifications selected by the user. The section 12b also calculates design parameters of the circuit patterns. The pattern selecting section 12c provides the user with the circuit patterns generated by the section 12b together with the design parameters thereof and causes the user to select one of the circuit patterns.

[0031]

The cell library 13 stores a plurality of standard cells for optimizing a circuit pattern for each functional unit. Combining these standard cells thus generates a circuit pattern.

[0032]

The CP aperture library 14 stores a plurality of CP apertures as design data, the CP apertures being used for electron-beam exposure in the CP (character projection) method. With the CP apertures stored in the CP aperture library 14, a circuit pattern can be designed by combining the VSB and CP methods.

[0033]

An operation of the semiconductor-device production system according to the first embodiment will now be described with reference to the timing chart shown in FIG. 3 and the flowchart shown in FIG. 4. Assume that in this operation, data is transferred through the network 5 unless otherwise specified.

[0034]

First, a user logs on to the server 1 from the user terminal 2 and requests the server 1 to produce a semiconductor device (s1). The condition setting section 12a of the processor 12 provides the user terminal 2 with a device operation/specification selecting screen, for example as shown in FIG. 5 (s2). In FIG. 5, reference numeral 41 indicates a list of a representative device and numerals 42, 43, and 44 denote an operating frequency, a chip area, and the number of products. The number of products can be designated by the number of chips, the number of wafers, the number of lots, and the like. It is desirable that the parameters of design specifications for specifying a user's desirable device, such as an operating frequency and a chip area, be input as not a uniquely-defined value but a value falling within a given range, e.g., 600 MHz to 620 MHz or 600 MHz or higher in the operating frequency. When the user describes an operation of the device in advance using hardware description language (HDL), the user can click a button "Upload" provided in the position of 41 in the screen shown in FIG. 5 and provide the server 1 with the operation. If the user clicks a button "OK," the input data is sent to the server 1 (s3). The user can thus advance to the next step (s4). If the user clicks a button "Cancel," the user can log off the server 1.

[0035]

The circuit pattern generating section 12b of the server 1 generates semiconductor-circuit patterns based on design specifications such as an operating frequency, a chip area, and the number of products transmitted from the user terminal 2 (s4).

[0036]

FIG. 6 is a flowchart showing a process of generating a semiconductor-circuit pattern in the circuit pattern generating section 12b (s4).

[0037]

Assume that a circuit pattern is formed by electron-beam exposure of the CP method. The generation of a pattern is tried using only the standard cells arranged on the CP apertures stored in the CP aperture library 14 (s41). The CP apertures stored in the CP aperture library 14 correspond to those mounted on the actual electron-beam exposure apparatus. Based on the stored CP apertures, information of standard cells prepared in the CP aperture can be acquired. In other words, a pattern is generated on the assumption that standard cells requiring a new CP aperture would not be used.

[0038]

When a plurality of CP apertures are stored in the CP aperture library 14, the generation in the above step (s41) is repeated by the number of combinations of the CP apertures. A pattern is thus formed for each of the combinations. It is thus determined whether a pattern is formed for each of the combinations (s42). If the generation for all the combinations is completed, the flow advances to step s43. If not, a pattern is generated for another combination again (s41).

[0039]

In step s43, logic synthesis and P & R are performed using all of the standard cells stored in the standard cell library 13 by the normal method, thereby forming a circuit pattern. With regard to a portion of the pattern exposed to an electron beam without using any CP aperture, the VSB method is adopted.

[0040]

In step s44, the number of shots required when the pattern formed in step s43 is exposed to an electron beam of the CP method is counted. In step s45, it is determined whether the formed circuit pattern is applicable to the registered CP aperture, and an inapplicable circuit pattern is assigned to a new CP aperture. Then, costs and periods required for producing the new CP aperture are calculated. It is then defined that one of the standard cells used in the pattern that produces the least effect of reducing the number of shots by the use of the CP method as compared with the use of the VSB method is not used for the next pattern generation (s46).

[0041]

The above operations of generating a pattern, counting the number of shots, and determining a standard cell that is not used next are repeated until a pattern which satisfies user's designated design specifications such as an operating frequency cannot be generated any more, and a pattern is generated in each operation. More specifically, it is determined every pattern generation whether the respective parameters of user's design specifications are satisfied or not (s47). If they are satisfied, the flow returns to step s43 and the number of shots for another generated pattern is counted. If not, the pattern generation ends (s48). In step s47, the parameters designated by the user are calculated for each generated pattern in the determination and the parameters are stored.

[0042]

A plurality of generated semiconductor-circuit patterns are obtained through the above operation. Design parameters as an operating frequency, a chip area, power consumption, a mask to be prepared or not, manufacturing costs and periods are calculated for each of the patterns (s5). The circuit pattern selecting section 12c displays a list of the generated patterns and the calculated design parameters on the screen of the user terminal 2 as shown in FIG. 7 (s6). The mask producing cost and period are calculated in consideration of the CP aperture preparing cost and period (s45).

[0043]

FIG. 8 is a graph showing an example of calculating design parameters of the consumption of power, the number of shots, the area of a chip in the case of decrement of the number of the standard cells. In this graph, the abscissa axis indicates the number of standard cells and the ordinate axis represents the chip area, power consumption and shot number that are normalized based on a pattern generated without restricting the use of standard cells. Referring to FIG. 8, a pattern is generated under the condition that the designed device can operate at a frequency of 100 MHz, and the number of characters usable in the electron-beam exposure apparatus of the CP method is 100 characters. In other words, the standard cells corresponding to 100 characters can be prepared on the CP aperture, and the part of the pattern which cannot be exposed by the standard cells are exposed by the VSB method.

[0044]

As shown in FIG. 8, the number of standard cells used when a circuit pattern is designed by a normal method is 84 different types, and the pattern is generated while gradually decreasing the number of standard cells used to generate the circuit. In FIG. 8, (A) indicates a pattern formed by a normal design method, (B) shows a pattern whose power consumption is the lowest, (C) represents a pattern the chip area of which is the smallest, (D) denotes a pattern in which the number of shots of an electron beam is sufficiently small and the increase of chip area and power consumption can be allowed, (E) indicates a pattern in which the number of shots of an electron beam is the smallest, and (F) denotes a pattern that can be formed only by a sufficiently small number of standard cells prepared on an already-registered (possessed) CP aperture. The circuit pattern generating section 12b of the server 1 obtains throughput of electron-beam exposure based on the number of shots of an electron beam for each pattern. The section 12b then obtains a manufacturing cost and period based on the throughput, the presence or absence of a CP aperture to be prepared, the number of lots of a semiconductor device to be manufactured, and the number of wafers.

[0045]

When the pattern (F) is selected and exposed to an electron beam using the already-existing or registered CP aperture, the chip area of the semiconductor device increases about 6% and its power consumption increases about 15% as compared with the normally-generated pattern (A), with the result that the semiconductor device deteriorates performance. Since the number of shots of an electron beam can be reduced in almost half and a new CP aperture need not be produced, a CP aperture manufacturing cost and period can be decreased. Of these patterns, the pattern (F) allows a device to be manufactured at lowest costs and highest speeds.

[0046]

A user determines whether a desired semiconductor-circuit pattern is included in a list of patterns with the above design parameters displayed as a criterion of determination (s6a). If the user determines that the desired pattern is included therein, the user clicks a check box on a screen corresponding to the pattern and selects the pattern. If the user then clicks an "OK" button, information of the selected pattern is sent to the server 1 (s7). The server 1 that received the selected-pattern information calculates the final cost of the selected pattern in order to place an order for devices with the pattern (s8). The server 1 transmits data on the cost to the user terminal 2 and displays it on the screen of the terminal 2 as shown in FIG. 9 and causes the user to input a payment method (s9). If the user is satisfied with the cost displayed on the screen shown in FIG. 9, the user inputs a payment method and then clicks the "OK" button. Then, the user officially places an order with the server 1 (s10). The server 1 thus places an order for devices with the device maker terminal 4, and transmits information about the pattern selected by the user (s11). If necessary, the server 1 requests the aperture maker terminal 3 to produce a new CP aperture (s12). Thus, the operation of receiving/placing an order for semiconductor devices is completed (s13).

[0047]

The device maker terminal 4 acquires data of a CP aperture for use from the CP aperture library 14 of the server 1. Based on the data, the device maker mounts the CP aperture corresponding to the data on the exposure apparatus and starts pattern exposure. If there is a request for producing a new CP aperture, the device maker mounts the CP aperture on the exposure apparatus which are provided from the aperture maker not through the network 5 and starts pattern exposure.

[0048]

If there are no patterns with which the user can be satisfied in step s6a, it is determined whether a design for the patterns should be changed by modifying design specification such as the operating frequency and chip area of the device in step s14. If the user wants to change the design, the user clicks a "Retry" button on the screen shown in FIG. 7 and returns to step s2 to input the conditions (design specifications) on the screen shown in FIG. 5 again. To complete the design, the user clicks the "Cancel" button to log off the server 1 (s13).

[0049]

According to the present embodiment, a user who makes a request to produce a semiconductor device can directly contact a server of a semiconductor maker through the network 5 and generate a circuit pattern of a desired device by simulation. In this case, the design parameters such as the performance of a device, the area of a chip, and the manufacturing costs and periods, which are required by the user as a criterion of determination for making a request to produce a device, are presented to and selected by the user. The user can thus select and order the most suitable pattern without causing a difference in consciousness among the designer, process engineer, and user. More specifically, though the performance of the device is slightly degraded, a pattern that allows the device to be produced inexpensively and quickly can be selected.

[0050]

Further, a manufacturing period, which varies with whether an existing CP aperture can be used for electron-beam exposure, can correctly be estimated. Since the use of the existing CP aperture is taken into consideration, the cost and period for manufacturing the CP aperture can be omitted, and the cost can be prevented from increasing even when a small number of devices are produced.

[0051]

Since, moreover, the server can place an order with a semiconductor maker and a CP aperture maker in real time, the manufacturing period can be shortened.

[0052]

The present invention is not limited to the above embodiment. For example, the aperture maker terminal 3 or the device maker terminal 4 need not be connected to the network 5 if only the server 1 and user terminal 2 are connected to the network 5. In this case, it is preferable that the device maker terminal 4 be connected to at least the CP aperture library 14 of the server 1 by a private line to receive data.

[0053]

The server 1 can also be used as a device maker. Specifically, the server 1 can receive an order from a user and produce a pattern based on information of the order as a device maker.

[0054]

FIG. 7 shows a list of parameters used when a user selects a desired one from among a plurality of circuit patterns. However, as shown in FIG. 8, each of the parameters can be indicated by a line graph that is normalized by a normal design method. Needless to say, the design parameters can be indicated by any other methods such as bar charts if they are presented to a user. In FIG. 7, the design parameters such as an operating frequency are each represented using a unit for actually determining a function of a semiconductor device by a user. However, as shown in FIG. 8, the parameters can be presented together with the normalized values, or only the normalized values can be presented. In this case, it is preferable that a design specification value of the operation and specification of a device provided by a user (s3) be set to 1.

[0055]

In the above embodiment, semiconductor devices are produced by electron-beam exposure. However, it is needless to say that they can be produced by other charged particle beam exposure such as ion-beam exposure.

[0056]

In the above embodiment, the VSB method is combined with the CP method. However, a method other than the VSB method can be used. For example, the other methods such as a so-called single-stroke method using a point beam can be combined with the CP method.

[0057]

According to the present invention, the transfer of information between a person who places an order (user) and a person who receives an order (server) need not always be performed through the network. For example, the server may calculate user's required design parameters regarding a plurality of circuit patterns and provides the user with a list of the design parameters by paper to cause the user to select a user's desired circuit pattern. It is thus confirmed that the present specification contains the following invention.

[0058]

A method of receiving an order for a semiconductor device and producing the semiconductor device based on information transferred between a person who wishes to receive an order and a person who wishes to place an order, comprises: a first step of causing the person who wises to place an order to provide specifications of the semiconductor device by request of the person who wishes to place an order; a second step of generating a plurality of circuit patterns in consideration of conditions for transferring a pattern by electron-beam exposure of a character projection method based on the specifications of the semiconductor device selected by the person who wishes to place an order, and obtaining at least two design parameters for each of the circuit patterns, and a third step of presenting the design parameters to the person who wishes to place an order for each of the circuit patterns and causing the person who wishes to place an order to select a circuit pattern satisfying a desired condition.

[0059]

[Advantage of the Invention]

As described in detail above, a semiconductor-device producing method according to the present invention allows a semiconductor device to be produced efficiently so as to fill the user's needs.

[Brief Description of the Drawings]

[FIG. 1]

A block diagram showing a network structure of a semiconductor-device production system according to a first embodiment of the present invention.

[FIG. 2]

A block diagram showing in detail an example of a server according to the embodiment.

[FIG. 3]

A timing chart showing an operation of the semiconductor-device production system according to the embodiment.

[FIG. 4]

A flowchart showing an operation of the semiconductor-device production system according to the embodiment.

[FIG. 5]

A view showing an example of a screen for selecting from among device operations and specifications displayed on a user terminal according to the embodiment.

[FIG. 6]

A flowchart showing a process of generating a semiconductor-circuit pattern in the server according to the embodiment.

[FIG. 7]

A view showing an example of a screen for selecting a pattern displayed on the user terminal according to the embodiment.

[FIG. 8]

A graph showing a relationship between the number of standard cells and the parameters of power consumption, the number of shots, and chip area when the number of standard cells decreases in the semiconductor-device production system according to the embodiment.

[FIG. 9]

A screen for placing an order displayed on the user terminal according to the embodiment.

[FIG. 10]

A flowchart showing a prior art process of producing a semiconductor device.

[Explanation of Reference Symbols]

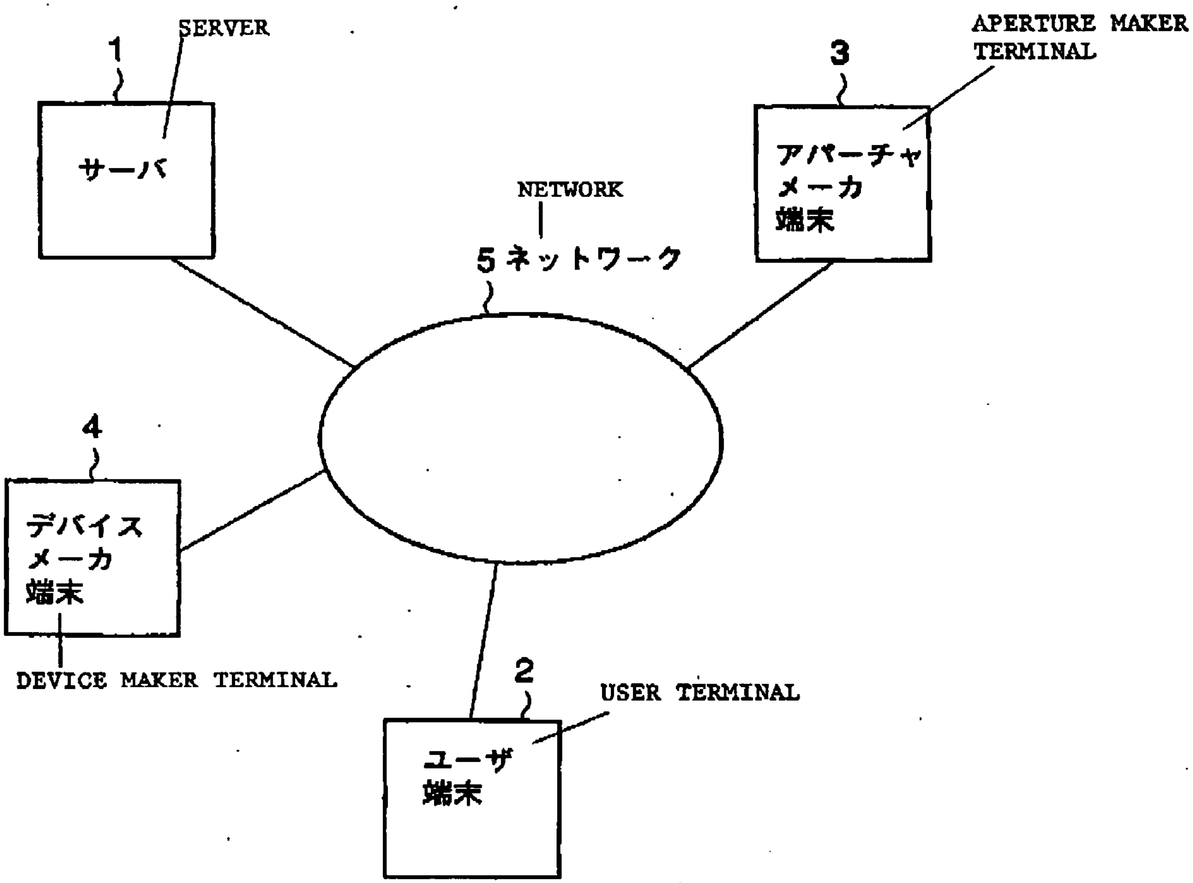
1: Server
2: User terminal
3: Aperture maker terminal
4: Device maker terminal
5: Network
11: Interface
12: Processor
12a: Condition setting section
12b: Circuit pattern generating section
12c: Circuit pattern selecting section
13: Cell library
14: CP aperture library

NAME OF DOCUMENT

【書類名】 図面 DRAWINGS

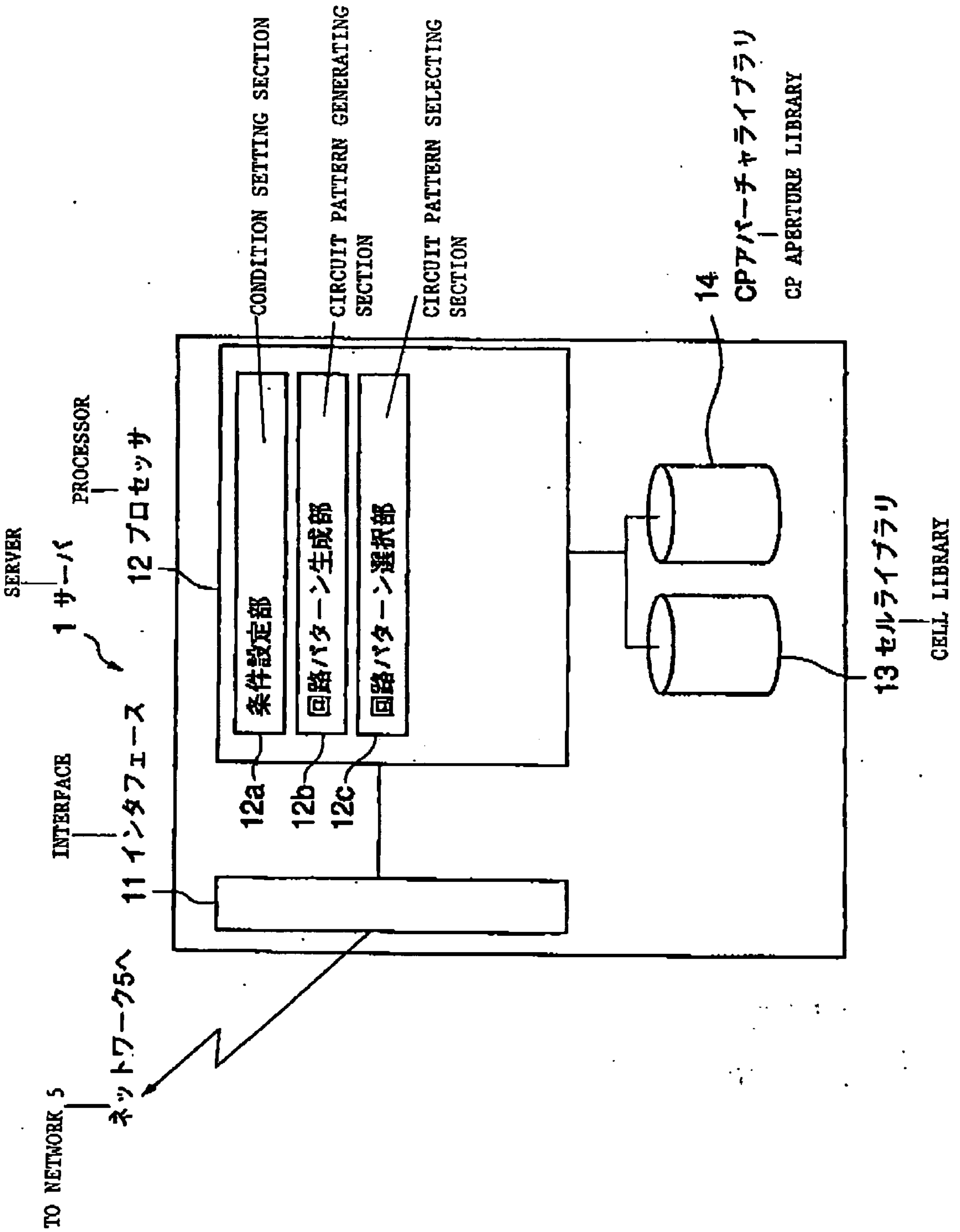
【図１】

FIG. 1


SERVER
1
サーバ
APERTURE MAKER TERMINAL
3
アパーチャメーカ端末
NETWORK
5 ネットワーク
4
デバイスメーカ端末
DEVICE MAKER TERMINAL
2
USER TERMINAL
ユーザ端末

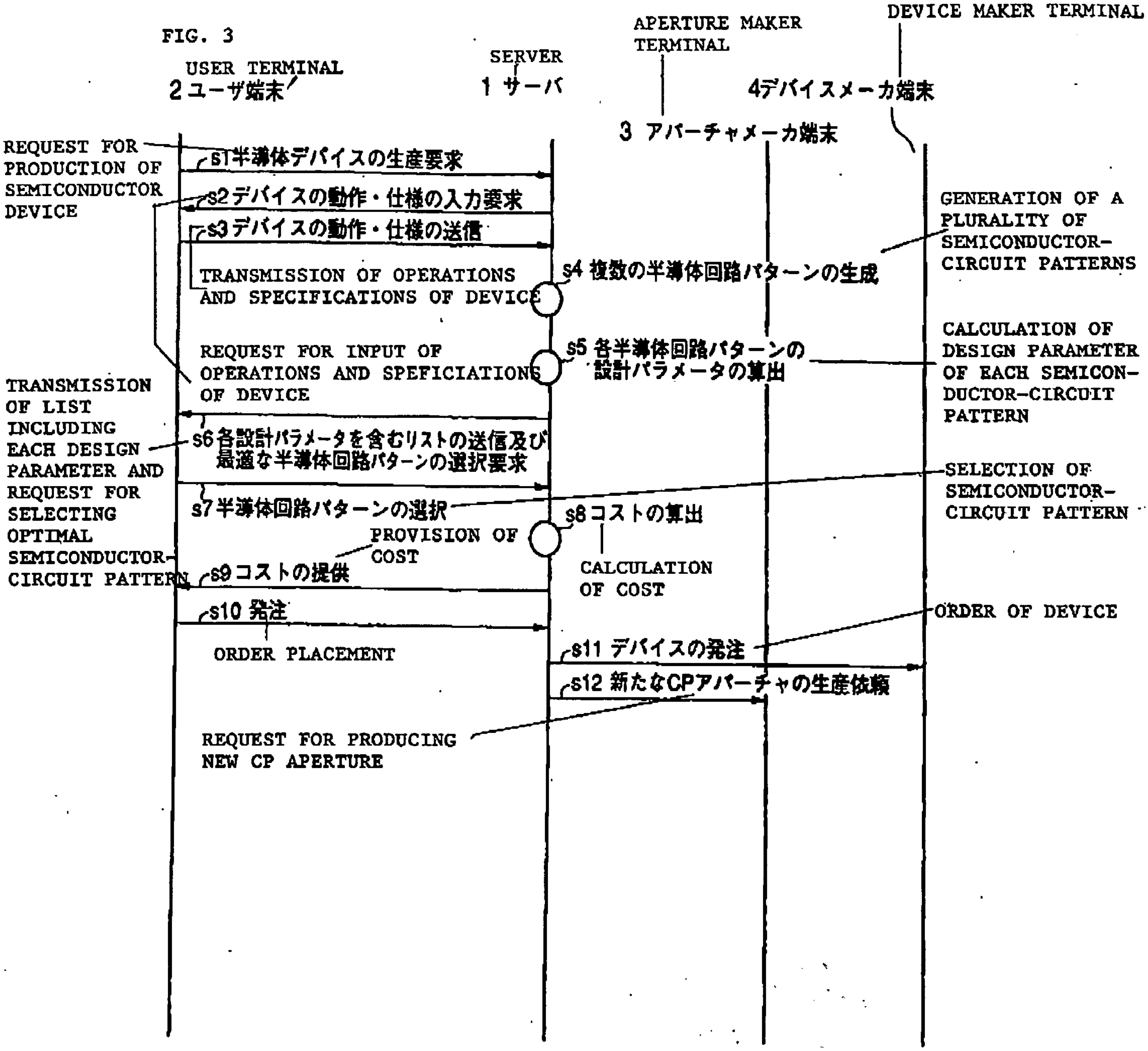
【図2】

FIG. 2


1 サーバ
SERVER
12 プロセッサ
PROCESSOR
11 インタフェース
INTERFACE
ネットワーク5へ
TO NETWORK 5
条件設定部
回路パターン生成部
回路パターン選択部
12a
12b
12c
CONDITION SETTING SECTION
CIRCUIT PATTERN GENERATING SECTION
CIRCUIT PATTERN SELECTING SECTION
14 CPアパーチャライブラリ
CP APERTURE LIBRARY
13 セルライブラリ
CELL LIBRARY

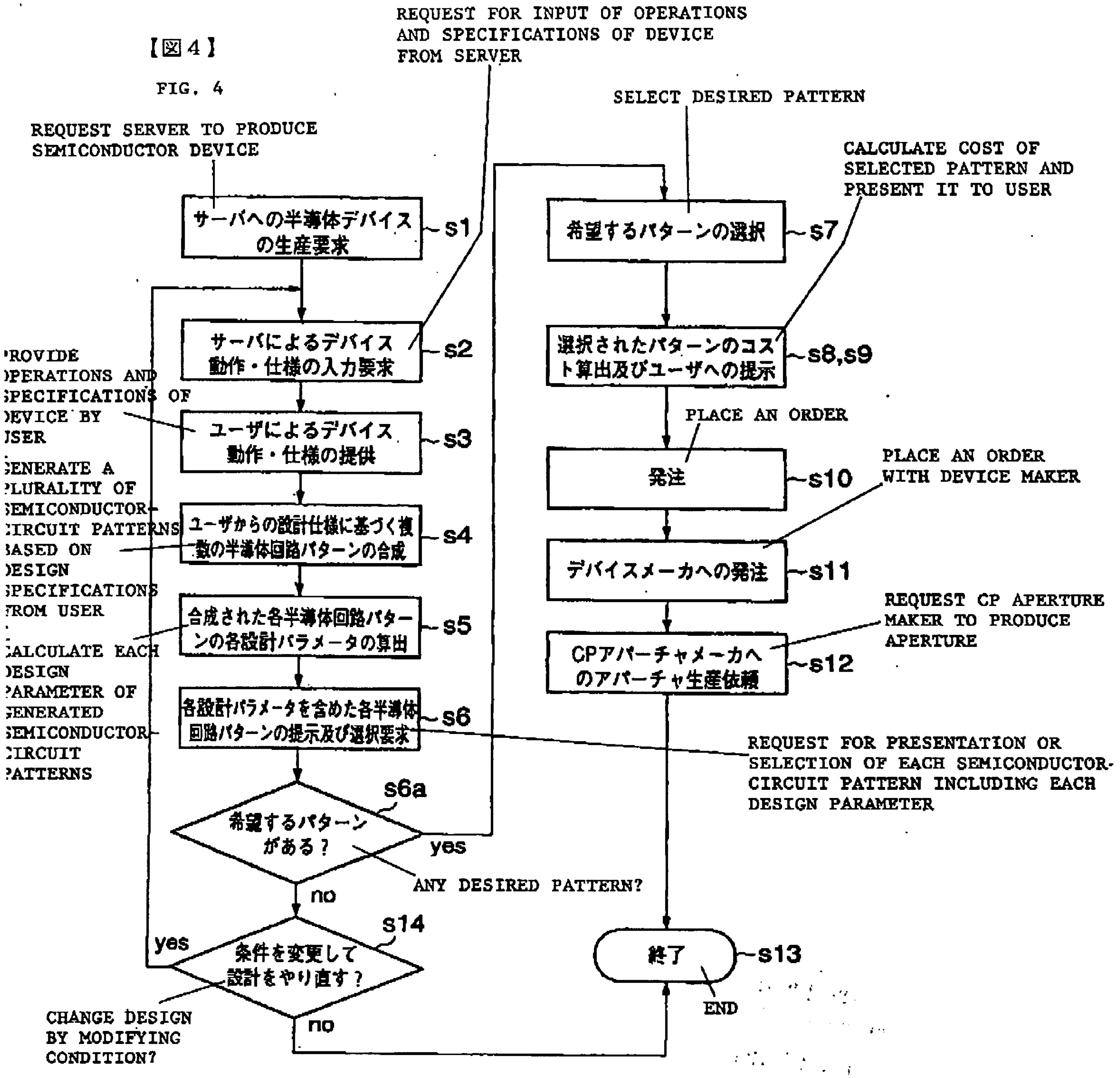
【図3】

FIG. 3


USER TERMINAL
2 ユーザ端末
SERVER
1 サーバ
APERTURE MAKER TERMINAL
3 アパーチャメーカ端末
DEVICE MAKER TERMINAL
4 デバイスメーカ端末
REQUEST FOR PRODUCTION OF SEMICONDUCTOR DEVICE
s1 半導体デバイスの生産要求
s2 デバイスの動作・仕様の入力要求
s3 デバイスの動作・仕様の送信
TRANSMISSION OF OPERATIONS AND SPECIFICATIONS OF DEVICE
s4 複数の半導体回路パターンの生成
GENERATION OF A PLURALITY OF SEMICONDUCTOR-CIRCUIT PATTERNS
REQUEST FOR INPUT OF OPERATIONS AND SPEFICIATIONS OF DEVICE
s5 各半導体回路パターンの設計パラメータの算出
CALCULATION OF DESIGN PARAMETER OF EACH SEMICONDUCTOR-CIRCUIT PATTERN
TRANSMISSION OF LIST INCLUDING EACH DESIGN PARAMETER AND REQUEST FOR SELECTING OPTIMAL SEMICONDUCTOR-CIRCUIT PATTERN
s6 各設計パラメータを含むリストの送信及び最適な半導体回路パターンの選択要求
s7 半導体回路パターンの選択
SELECTION OF SEMICONDUCTOR-CIRCUIT PATTERN
s8 コストの算出
PROVISION OF COST
CALCULATION OF COST
s9 コストの提供
s10 発注
ORDER PLACEMENT
s11 デバイスの発注
ORDER OF DEVICE
s12 新たなCPアパーチャの生産依頼
REQUEST FOR PRODUCING NEW CP APERTURE

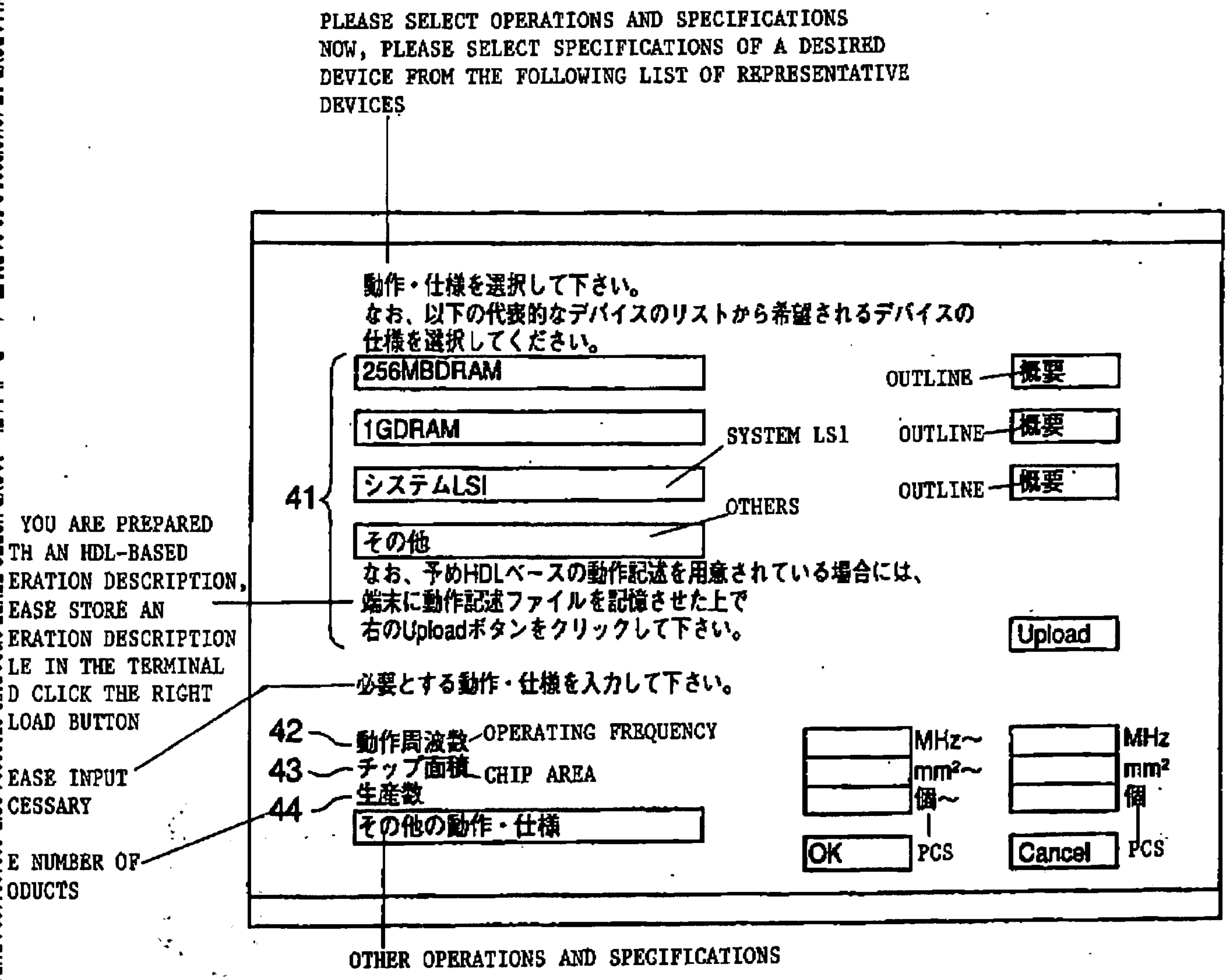
【図4】

FIG. 4


REQUEST FOR INPUT OF OPERATIONS AND SPECIFICATIONS OF DEVICE FROM SERVER
REQUEST SERVER TO PRODUCE SEMICONDUCTOR DEVICE
サーバへの半導体デバイスの生産要求
s1
サーバによるデバイス動作・仕様の入力要求
s2
ROVIDE PERATIONS AND PECIFICATIONS OF EVICE BY SER
ユーザによるデバイス動作・仕様の提供
s3
ENERATE A LURALITY OF EMICONDUCTOR-IRCUIT PATTERNS ASED ON ESIGN PECIFICATIONS ROM USER
ユーザからの設計仕様に基づく複数の半導体回路パターンの合成
s4
ALCULATE EACH ESIGN ARAMETER OF ENERATED EMICONDUCTOR-IRCUIT ATTERNS
合成された各半導体回路パターンの各設計パラメータの算出
s5
各設計パラメータを含めた各半導体回路パターンの提示及び選択要求
s6
REQUEST FOR PRESENTATION OR SELECTION OF EACH SEMICONDUCTOR-CIRCUIT PATTERN INCLUDING EACH DESIGN PARAMETER
s6a
希望するパターンがある？
yes
no
ANY DESIRED PATTERN?
s14
yes
条件を変更して設計をやり直す？
no
CHANGE DESIGN BY MODIFYING CONDITION?
SELECT DESIRED PATTERN
希望するパターンの選択
s7
CALCULATE COST OF SELECTED PATTERN AND PRESENT IT TO USER
選択されたパターンのコスト算出及びユーザへの提示
s8,s9
PLACE AN ORDER
発注
s10
PLACE AN ORDER WITH DEVICE MAKER
デバイスメーカへの発注
s11
REQUEST CP APERTURE MAKER TO PRODUCE APERTURE
CPアパーチャメーカへのアパーチャ生産依頼
s12
終了
s13
END

【図5】

FIG. 5


動作・仕様を選択して下さい。
なお、以下の代表的なデバイスのリストから希望されるデバイスの仕様を選択してください。

PLEASE SELECT OPERATIONS AND SPECIFICATIONS
NOW, PLEASE SELECT SPECIFICATIONS OF A DESIRED DEVICE FROM THE FOLLOWING LIST OF REPRESENTATIVE DEVICES

なお、予めHDLベースの動作記述を用意されている場合には、端末に動作記述ファイルを記憶させた上で右のUploadボタンをクリックして下さい。

YOU ARE PREPARED
TH AN HDL-BASED
ERATION DESCRIPTION,
EASE STORE AN
ERATION DESCRIPTION
LE IN THE TERMINAL
D CLICK THE RIGHT
LOAD BUTTON

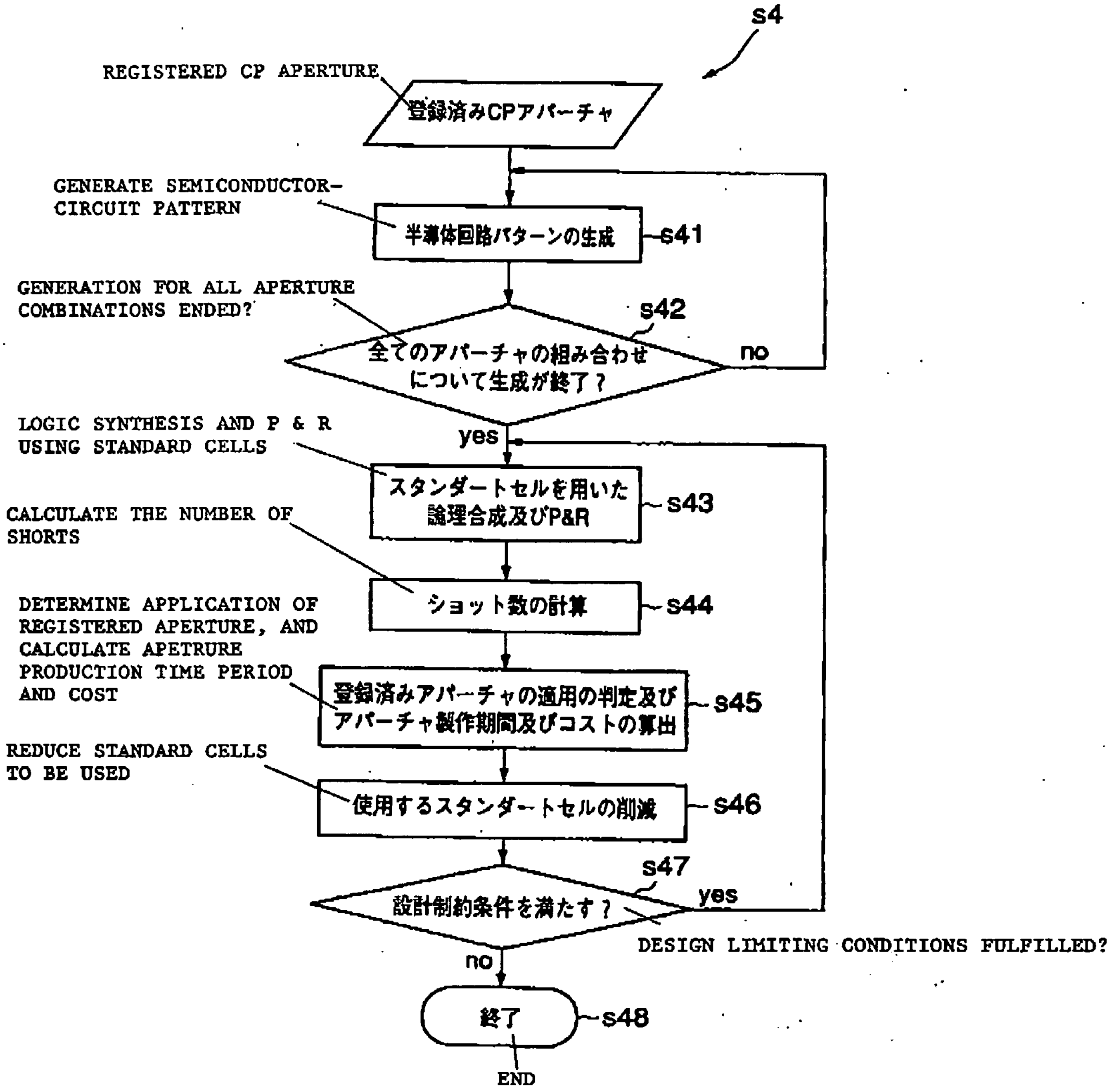
必要とする動作・仕様を入力して下さい。

EASE INPUT
CESSARY

256MBDRAM
1GDRAM
システムLSI
SYSTEM LS1
その他
OTHERS
41
OUTLINE
概要
OUTLINE
概要
OUTLINE
概要
Upload
42
動作周波数
OPERATING FREQUENCY
43
チップ面積
CHIP AREA
44
生産数
E NUMBER OF
ODUCTS
その他の動作・仕様
OTHER OPERATIONS AND SPECIFICATIONS
MHz～
mm²～
個～
PCS
MHz
mm²
個
PCS
OK
Cancel

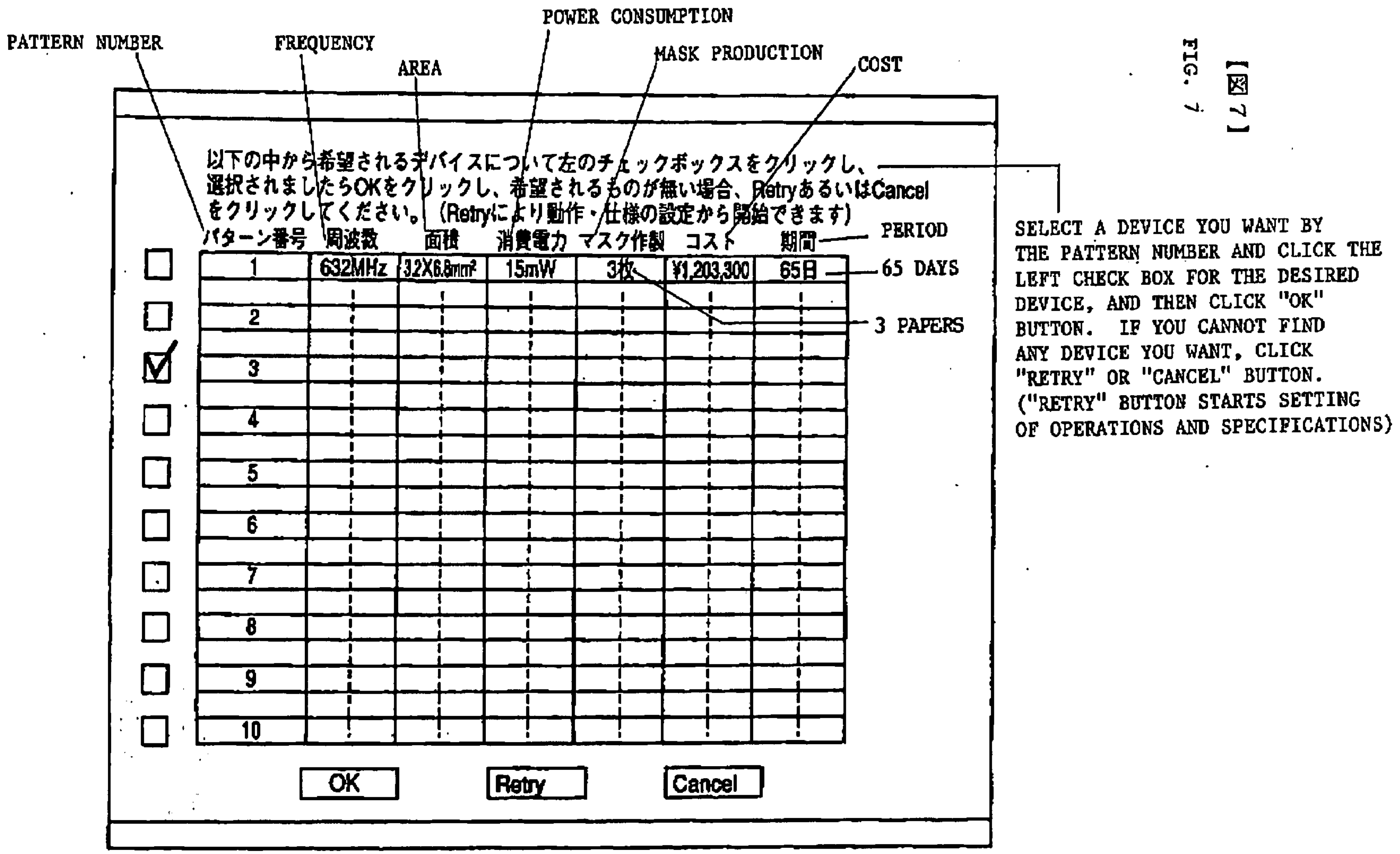
【図6】

FIG. 6


s4
REGISTERED CP APERTURE
登録済みCPアパーチャ
GENERATE SEMICONDUCTOR-CIRCUIT PATTERN
半導体回路パターンの生成
s41
GENERATION FOR ALL APERTURE COMBINATIONS ENDED?
s42
全てのアパーチャの組み合わせについて生成が終了？
no
yes
LOGIC SYNTHESIS AND P & R USING STANDARD CELLS
スタンダードセルを用いた論理合成及びP&R
s43
CALCULATE THE NUMBER OF SHORTS
ショット数の計算
s44
DETERMINE APPLICATION OF REGISTERED APERTURE, AND CALCULATE APETRURE PRODUCTION TIME PERIOD AND COST
登録済みアパーチャの適用の判定及びアパーチャ製作期間及びコストの算出
s45
REDUCE STANDARD CELLS TO BE USED
使用するスタンダードセルの削減
s46
s47
設計制約条件を満たす？
yes
DESIGN LIMITING CONDITIONS FULFILLED?
no
終了
s48
END

【図7】

FIG. 7


PATTERN NUMBER
FREQUENCY
AREA
POWER CONSUMPTION
MASK PRODUCTION
COST
PERIOD
65 DAYS
3 PAPERS
OK
Retry
Cancel

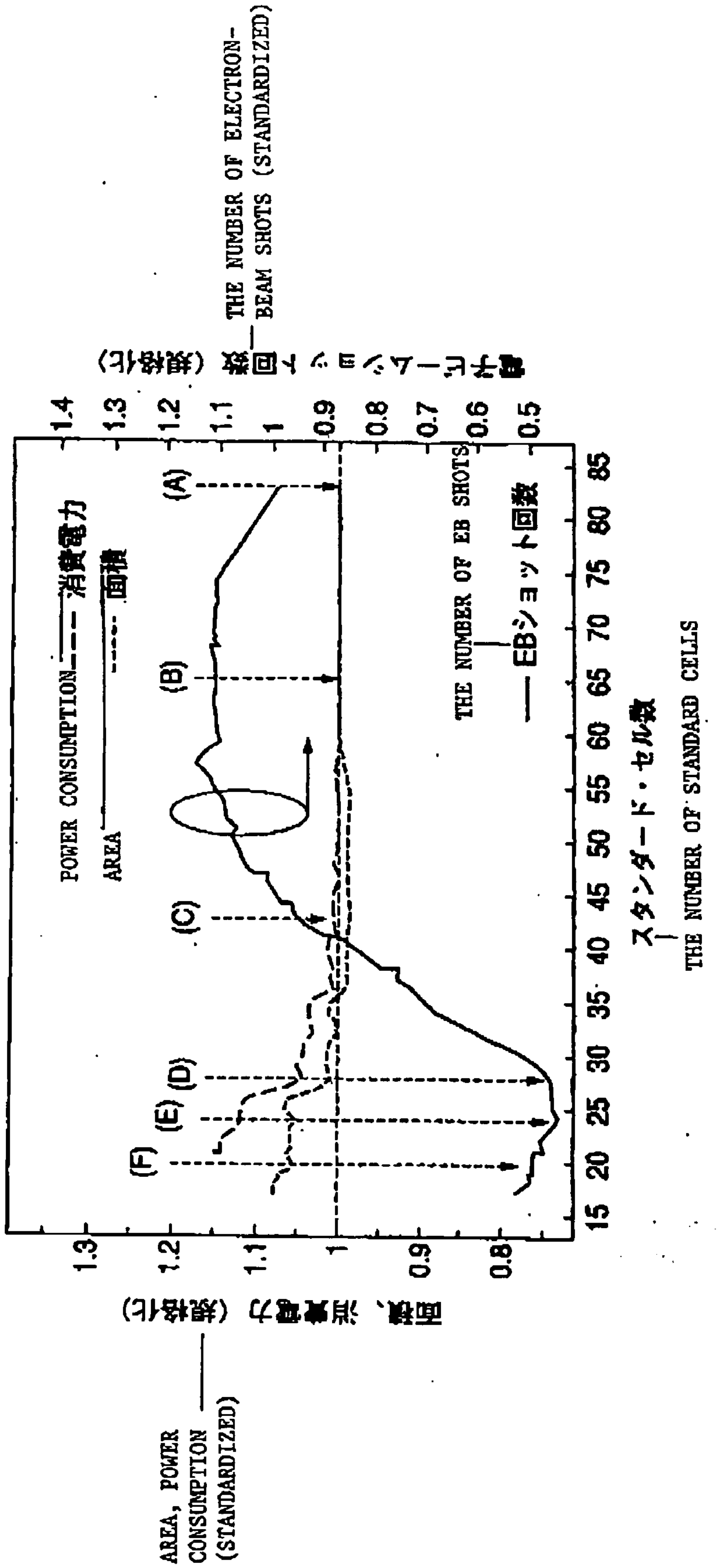
以下の中から希望されるデバイスについて左のチェックボックスをクリックし、選択されましたらOKをクリックし、希望されるものが無い場合、RetryあるいはCancelをクリックしてください。（Retryにより動作・仕様の設定から開始できます）

	パターン番号	周波数	面積	消費電力	マスク作製	コスト	期間
☐	1	632MHz	32X6.8mm²	15mW	3枚	¥1,203,300	65日
☐	2						
☑	3						
☐	4						
☐	5						
☐	6						
☐	7						
☐	8						
☐	9						
☐	10						

SELECT A DEVICE YOU WANT BY THE PATTERN NUMBER AND CLICK THE LEFT CHECK BOX FOR THE DESIRED DEVICE, AND THEN CLICK "OK" BUTTON. IF YOU CANNOT FIND ANY DEVICE YOU WANT, CLICK "RETRY" OR "CANCEL" BUTTON. ("RETRY" BUTTON STARTS SETTING OF OPERATIONS AND SPECIFICATIONS)

【図８】

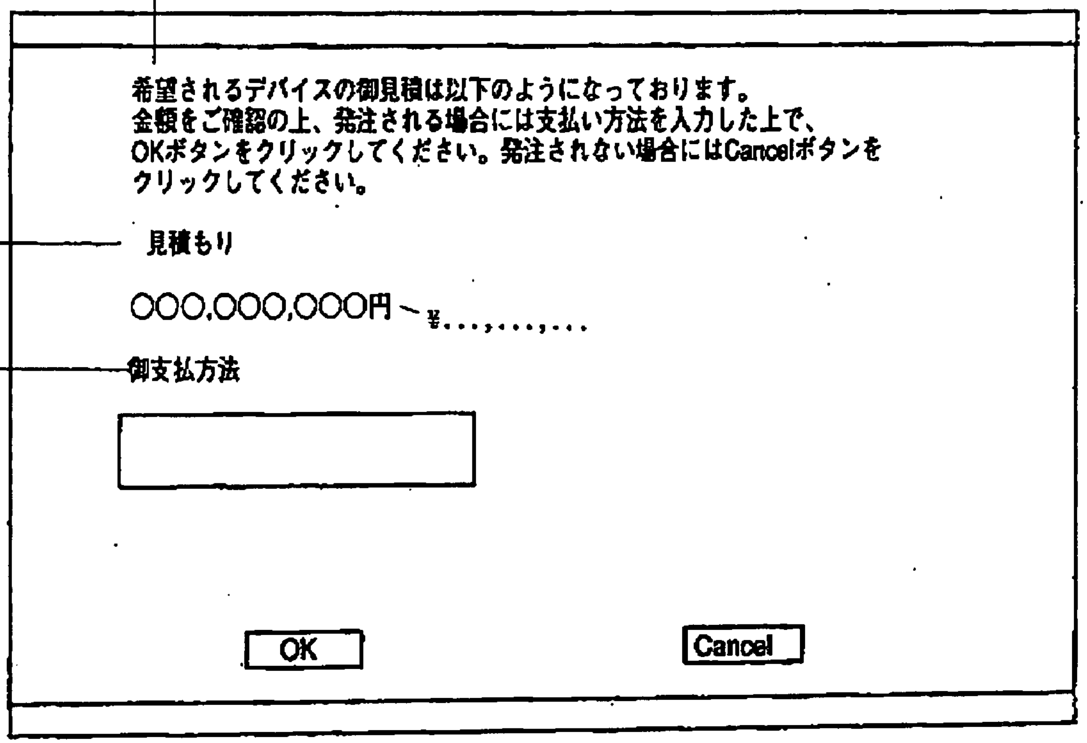
FIG. 8


電子ビームショット回数（規格化）
THE NUMBER OF ELECTRON-BEAM SHOTS (STANDARDIZED)
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
POWER CONSUMPTION
消費電力
AREA
面積
THE NUMBER OF EB SHOTS
EBショット回数
(A)
(B)
(C)
(D)
(E)
(F)
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
スタンダード・セル数
THE NUMBER OF STANDARD CELLS
1.3
1.2
1.1
1
0.9
0.8
面積、消費電力（規格化）
AREA, POWER CONSUMPTION (STANDARDIZED)

【図９】

FIG. 9

OUR QUOTATION FOR THE DEVICE YOU DESIRE IS STATED BELOW. CHECK THE PRICE. IF YOU WANT TO PLACE AN ORDER, INPUT A METHOD OF PAYMENT AND CLICK THE "OK" BUTTON. IF YOU DO NOT WANT TO PLACE AN ORDER, CLICK THE "CANCEL" BUTTON.



希望されるデバイスの御見積は以下のようになっております。
金額をご確認の上、発注される場合には支払い方法を入力した上で、
OKボタンをクリックしてください。発注されない場合にはCancelボタンをクリックしてください。

見積もり

OOO,OOO,OOO円～¥...,...,...

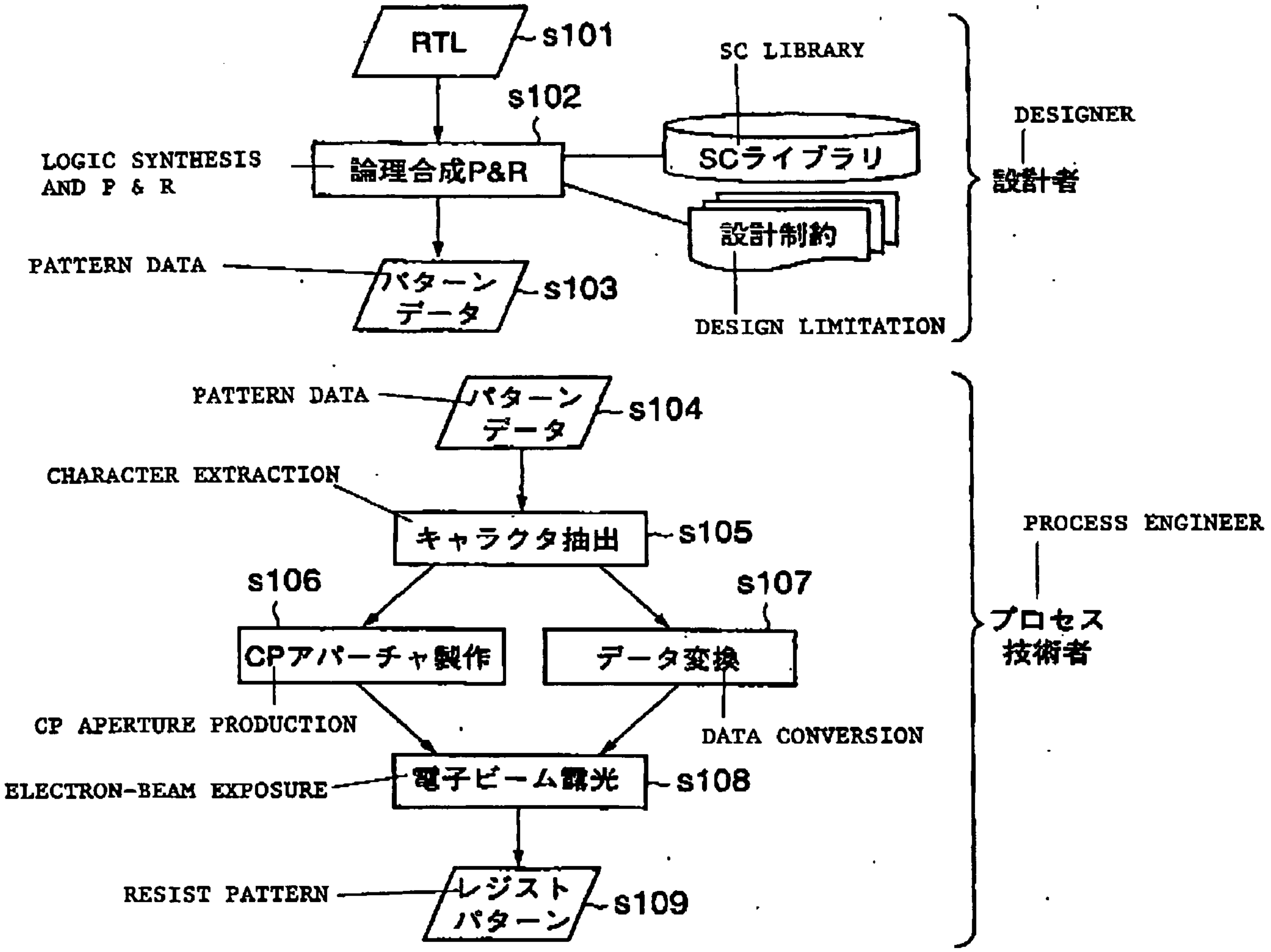
御支払方法

QUOTATION

METHOD OF PAYMENT

【図１０】

FIG. 10


RTL
s101
SC LIBRARY
s102
DESIGNER
LOGIC SYNTHESIS AND P & R
論理合成P&R
SCライブラリ
設計者
設計制約
PATTERN DATA
パターンデータ
s103
DESIGN LIMITATION
PATTERN DATA
パターンデータ
s104
CHARACTER EXTRACTION
キャラクタ抽出
s105
PROCESS ENGINEER
s106
s107
プロセス技術者
CPアパーチャ製作
データ変換
CP APERTURE PRODUCTION
DATA CONVERSION
ELECTRON-BEAM EXPOSURE
電子ビーム露光
s108
RESIST PATTERN
レジストパターン
s109

[Document] ABSTRACT

[Abstract]

[Object] To efficiently produce a semiconductor device that meets the user's needs.

[Means for Achieving the Object] A user is requested (s2) to input specifications of a semiconductor device in accordance with a request from the user (s1). Based on the specifications provided by the user (s3), a plurality of circuit patterns are generated by a CP method (s4), and a design parameter is calculated for each of the circuit patterns (s5). The user is provided with information of the plurality of circuit patterns together with the design parameters (s6) for circuit pattern selection. The user selects a desired circuit pattern (s7), whereas the server calculates manufacturing costs of the device (s8) and presents them to the user (s9). The user checks the costs and then places an order (s10).

[Elected Figure] FIG. 3